Single Channel, 1% Resistor tolerance, 1024/256-Position Digital Variable Resistor

Preliminary Technical Data

AD5272/AD5274

FEATURES

Single-channel, 1,024/256-position resolution
20 kΩ, 50 kΩ and 100 kΩ nominal resistance
Calibrated 1% Nominal Resistor Tolerance
Multiple-time programmable set-and-forget resistance setting allows 50 time permanent programming
Rheostat mode temperature coefficient: 35 ppm/°C
2.7V to 5.5V single-supply operation
±2.5V to ±2.75V dual-supply operation for AC or Bipolar Operations
I²C®-compatible interface
Wiper setting readback
Power-on refreshed from 50-TP memory
Thin LFCSP(SON)-10 (3 mm x 3 mm x 0.8 mm) package
Compact MSOP-10 (3 mm × 4.9 mm x 1.1mm) package

APPLICATIONS

Mechanical potentiometer replacement
Instrumentation: gain, offset adjustment
Programmable voltage to current conversion
Programmable filters, delays, time constants
Programmable power supply
Sensor calibration

FUNCTIONAL BLOCK DIAGRAM

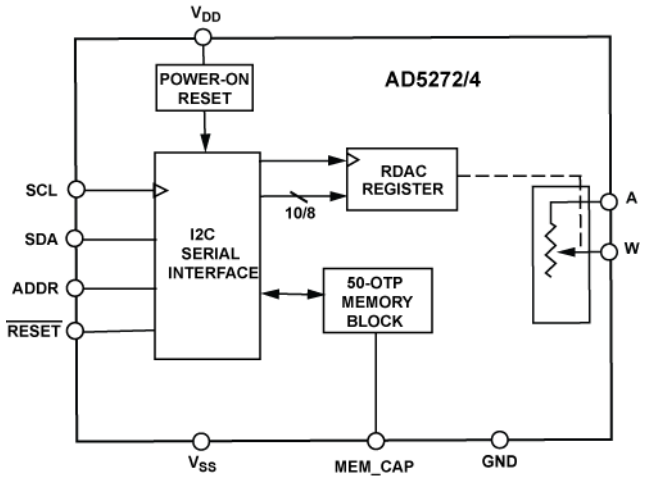

Figure 1. Block Diagram

GENERAL DESCRIPTION

The AD5272/4 are single-channel, 1024/256-positions digitally controlled resistors[1] with less than 1% end-to-end Resistor Tolerance error and 50-Time Programmable Memory. The AD5272/4 perform the same electronic adjustment function as a mechanical rheostat with enhanced resolution, solid state reliability, and superior low temperature coefficient performance.

The AD5272/4 offer guaranteed industry leading low resistor tolerance errors of ±1% with a nominal temperature coefficient of 35 ppm/°C. The low resistor tolerance feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5272/4 device wiper settings are controllable through the I²C compatible digital interface. Unlimited adjustments are allowed before programming the resistance value into the 50-TP (50-Time Programmable) memory. The AD5272/4 do not require any external voltage supply to facilitate fuse blow and there are 50 opportunities for permanent programming. During 50-TP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

The AD5272 and AD5274 are available in a thin 3mmX3mm LFCSP package and in a compact 10ld MSOP package. The parts are guaranteed to operate over the extended industrial temperature range of −40°C to +105°C.

[1] The terms programmable resistor and RDAC are used interchangeably.

Rev. PrA

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS – 50KΩ AND 100KΩ VERSIONS

V_{DD} = 2.7V to 5.5V, V_{SS} = 0V; V_{DD} = 2.5V to 2.75V, V_{SS} = -2.5V to -2.75V; −40°C < T_A < +105°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS— RHEOSTAT MODE					
Resolution					Bits
AD5272		10			
AD5274		8			
Resistor Integral Nonlinearity[2]					LSB
AD5270	V_{DD} = 3.0V to 5.5V	−1		+1	LSB
	V_{DD} = 2.7V to 3.0V	−1		+1.5	
AD5271		-1		+1	
Resistor Differential Nonlinearity[2]		−1		+1	LSB
Nominal Resistor Tolerance[3]		−1	0.5	+1	%
Resistance Temperature Coefficient			35		ppm/°C
Wiper Resistance			35	70	Ω
RESISTOR TERMINALS					
Terminal Voltage Range[4]		V_{SS}		V_{DD}	V
Capacitance[5] A	f = 1 MHz, measured to GND, Code = half-scale		165		pF
Capacitance[5] W	f = 1 MHz, measured to GND, Code = half-scale		60		pF
Common-Mode Leakage Current[5]	$V_A = V_W$			4	nA
DIGITAL INPUTS					
V_{INH}, Input Logic High	V_{DD} = 2.7V to 5.5 V, V_{SS} = 0V,	0.7xV_{DD}			V
	V_{DD} = 2.5V, V_{SS} = -2.5V	2.4V			V
V_{INL}, Input Logic Low				0.3xV_{DD}	V
V_{HYST}, Input Hysteresis		0.1XV_{DD}			V
I_{IN}, Input Current				±1	µA
C_{IN},Input Capacitance[5]			5		pF
DIGITAL OUTPUTS(OPEN DRAIN)					
V_{OL}, Output Low Voltage[6]	I_{SINK} = 3mA			0.4	V
	I_{SINK} = 6mA			0.6	V
Three state Leakage Current		-1		1	µA
Three state Output Capacitance[5]			2		pF
POWER SUPPLIES					
Single-Supply Power Range	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range		±2.5		±2.75	V
I_{DD}, Positive Supply Current				1	µA
I_{SS}, Negative Supply Current				-1	µA
$I_{DD\_OTP\_STORE}$, OTP Store Current[5,7]				4	mA
$I_{SS\_OTP\_STORE}$, OTP Store Current[5,7]				-4	mA
$I_{DD\_OTP\_READ}$, OTP Read Current[5,8]				500	µA
$I_{SS\_OTP\_READ}$, OTP Read Current[5,8]				-500	µA
Power Dissipation[9]	$V_{IH} = V_{DD}$ or V_{IL} = GND			11	mW
Power Supply Rejection Ratio[5]	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%		-90	-60	dB
DYNAMIC CHARACTERISTICS[5, 10]					
Bandwidth	−3 dB,				kHz
	R_{AW} = 50 kΩ		20		
	R_{AW} = 100 kΩ		10		

Parameter	Conditions	Min	Typ[1]	Max	Unit
Total Harmonic Distortion	V_A = 1 V rms, f = 1 kHz				
	R_{AW} = 50 kΩ		-60		dB
	R_{AW} = 100 kΩ		-57		
Resistor Noise Density	R_{WB} = 5 kΩ, T_A = 25°C,		9.2		nV/√Hz

[1] Typicals represent average readings at 25°C,V_{DD} = 5 V and V_{SS} = 0 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] ±1% resistor tolerance code range per end-to-end resistor option;
AD5272: R_{AB} = 50KΩ: 50 to 1,023 for $|V_{DD} - V_{SS}|$ = 4.5V to 5.5V, 85 to 1,023 for $|V_{DD} - V_{SS}|$ = 3V to 4.5V and TBD to 1,023 for $|V_{DD} - V_{SS}|$ = 2.7V to 2.9V;
R_{AB} = 100kΩ: 20 to 1,023 for $|V_{DD} - V_{SS}|$ = 4.5V to 5.5V, 75 to 1,023 for $|V_{DD} - V_{SS}|$ = 3V to 4.5V and TBD to 1,023 for $|V_{DD} - V_{SS}|$ = 2.7V to 2.9V.
AD5274: R_{AB} = 50KΩ: 12 to 255 for $|V_{DD} - V_{SS}|$ = 4.5V to 5.5V, 22 to 255 for $|V_{DD} - V_{SS}|$ = 3V to 4.5V and TBD to 255 for $|V_{DD} - V_{SS}|$ = 2.7V to 2.9V;
R_{AB} = 100KΩ: 5 to 255 for $|V_{DD} - V_{SS}|$ = 4.5V to 5.5V, 19 to 255 for $|V_{DD} - V_{SS}|$ = 3V to 4.5V and TBD to 255 for $|V_{DD} - V_{SS}|$ = 2.7V to 2.9V.
[4] Resistor Terminals A and W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[5] Guaranteed by design and not subject to production test.
[6] Max I_{SINK} = 3mA in bipolar mode(V_{SS} < 0V)
[7] Different from operating current; supply current for fuse program lasts approximately TBDµs.
[8] Different from operating current; supply current for fuse read lasts approximately TBDµs..
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).
[10] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

ELECTRICAL CHARACTERISTICS – 20KΩ

V_{DD} = 2.7V to 5.5V, V_{SS} = 0V; V_{DD} = 2.5V to 2.75V, V_{SS} = -2.5V to -2.75V; −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS— RHEOSTAT MODE					
Resolution					Bits
AD5272		10			
AD5274		8			
Resistor Integral Nonlinearity[2]					
AD5272	V_{DD} = 4.5V to 5.5V	−1		+1	LSB
	V_{DD} = 3.0V to 4.4V	−1.5		+2	LSB
	V_{DD} = 2.7V to 3.0V		±1.75		LSB
AD5274		−1		+1	
Resistor Differential Nonlinearity[2]		−1		+1	LSB
Nominal Resistor Tolerance[3]		−1	0.5	+1	%
Resistance Temperature Coefficient			35		ppm/°C
Wiper Resistance			35	70	Ω
RESISTOR TERMINALS					
Terminal Voltage Range[4]		V_{SS}		V_{DD}	V
Capacitance[5] A	f = 1 MHz, measured to GND, Code = half-scale		165		pF
Capacitance[5] W	f = 1 MHz, measured to GND, Code = half-scale		60		pF
Common-Mode Leakage Current[5]	$V_A = V_W$			4	nA
DIGITAL INPUTS					
V_{INH}, Input Logic High	V_{DD} = 2.7V to 5.5 V,V_{SS} = 0V,	0.7xV_{DD}			V
	V_{DD} = 2.5V,V_{SS} = -2.5V	2.4V			V
V_{INL}, Input Logic Low				0.3xV_{DD}	V
V_{HYST}, Input Hysteresis		0.1XV_{DD}			V
I_{IN}, Input Current				±1	µA
C_{IN},Input Capacitance[5]			5		pF
DIGITAL OUTPUTS(OPEN DRAIN)					
V_{OL}, Output Low Voltage[6]	I_{SINK} = 3mA;			0.4	V
	I_{SINK} = 6mA			0.6	V
Three state Leakage Current		-1		1	µA
Three state Output Capacitance[5]			2		pF
POWER SUPPLIES					
Single-Supply Power Range	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range		±2.5		±2.75	V
I_{DD}, Positive Supply Current				1	µA
I_{SS}, Negative Supply Current				-1	µA
$I_{DD\_OTP\_STORE}$, OTP Store Current[5,7]				4	mA
$I_{SS\_OTP\_STORE}$, OTP Store Current[5,7]				-4	mA
$I_{DD\_OTP\_READ}$, OTP Read Current[5,8]				500	µA
$I_{SS\_OTP\_READ}$, OTP Read Current[5,8]				-500	µA
Power Dissipation[9]	$V_{IH} = V_{DD}$ or V_{IL} = GND			16.5	mW
Power Supply Rejection Ratio[5]	$\Delta V_{DD}/\Delta V_{SS}$ = 5 V ± 10%		-80	-50	dB
DYNAMIC CHARACTERISTICS[5, 10]					
Bandwidth	−3 dB,				
	R_{AW} = 20 kΩ		50		kHz

Parameter	Conditions	Min	Typ[1]	Max	Unit
Total Harmonic Distortion	V_A = 1 V rms, f = 1 kHz				
	R_{AW} = 20 kΩ		70		dB
Resistor Noise Density	R_{WB} = 5 kΩ, T_A = 25°C,		9.2		nV/√Hz

[1] Typicals represent average readings at 25°C,V_{DD} = 5 V and V_{SS} = 0 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] ±1% resistor tolerance code range per end-to-end resistor option;
AD5272: R_{AB} = 20KΩ: 18 to 1,023 for $|V_{DD} - V_{SS}|$ = 4.5V to 5.5V, 270 to 1,023 for $|V_{DD} - V_{SS}|$ = 3V to 4.5V and TBD to 1,023 for $|V_{DD} - V_{SS}|$ = 2.7V to 2.9V;
AD5274: R_{AB} = 20KΩ: 70 to 255 for $|V_{DD} - V_{SS}|$ = 4.5V to 5.5V, 68 to 255 for $|V_{DD} - V_{SS}|$ = 3V to 4.5V and TBD to 255 for $|V_{DD} - V_{SS}|$ = 2.7V to 2.9V;
[4] Resistor Terminals A and W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
[5] Guaranteed by design and not subject to production test.
[6] Max I_{SINK} = 3mA in bipolar mode(V_{SS}<0V).
[7] Different from operating current; supply current for fuse program lasts approximately TBDµs.
[8] Different from operating current; supply current for fuse read lasts approximately TBDµs..
[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).
[10] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

INTERFACE TIMING SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Conditions[1]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
f_{SCL}[2]	Standard mode		100	KHz	Serial clock frequency
	Fast mode		400	KHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
t_5	Standard mode	4.7		µs	$t_{SU;STA,}$ set-up time for a repeated start condition
	Fast mode	0.6		µs	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
	High speed mode	160		ns	
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
t_{12}	$\overline{\text{RESET}}$ Pulse Time	TBD		ns	Minimum $\overline{\text{RESET}}$ low time
t_{SP}[3]	Fast mode	0	50	ns	Pulse width of spike suppressed
t_{OTP}			TBD	ms	Power-on OTP restore time
$t_{MEMORY\_PROGRAM}$			TBD	ms	Memory Program Time
t_{MEMORY_READ}			TBD	ms	Memory Read Time

[1] C_B refers to the capacitance on the bus line.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.
[3] Input filtering on the SCL and SDA inputs suppress noise spikes that are less than 50 ns for fast mode.

TIMING DIAGRAM

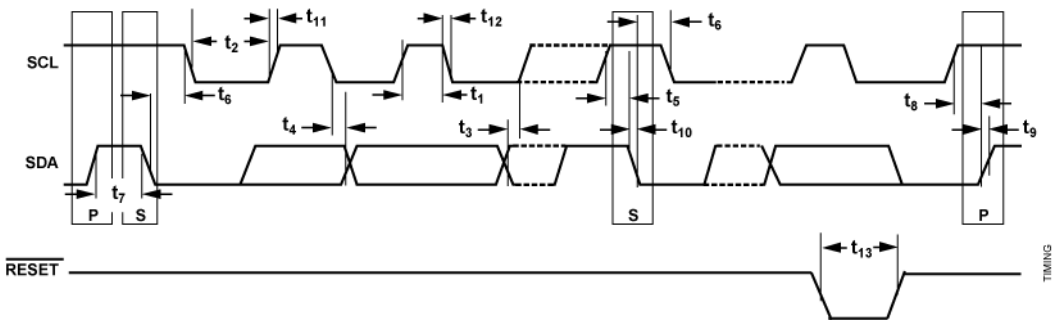

Figure 2. 2-Wire Serial Interface Timing Diagram

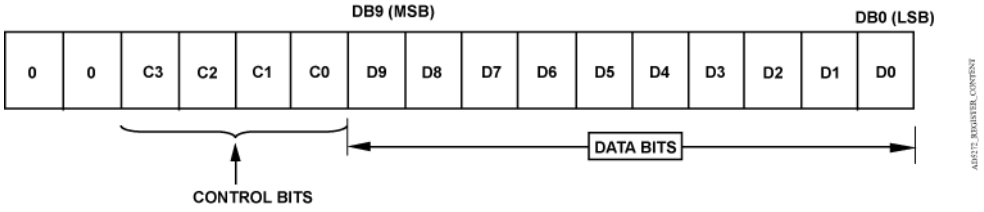

Figure 3. AD5272 Input Register Content

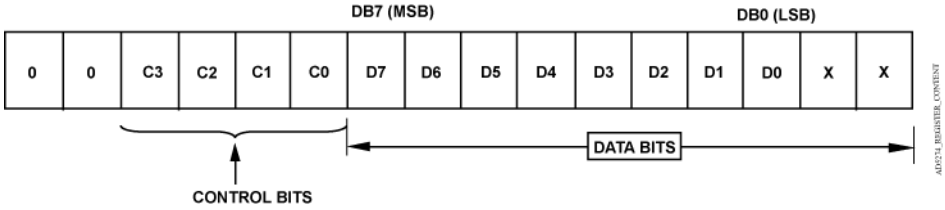

Figure 4. AD5274 Input Register Content

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7.0 V
V_{SS} to GND	+0.3 V, –7.0 V
V_{DD} to V_{SS}	7 V
V_A, V_W to GND	V_{SS}–0.3 V to V_{DD}+0.3 V
I_A, I_W	
Pulsed[1]	±TBD mA
Continuous	
20KΩ End-to-End resistance	±3 mA
50KΩ and 100 KΩ End-to-End resistance	±2 mA
Digital Inputs SDA and SCL	-0.3 V to +7.0 V
Digital Inputs AD0 and $\overline{\text{RESET}}$	-0.3 V to V_{DD} +0.3 V
Operating Temperature Range[2]	–40°C to +125°C
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature	–65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at peak temperature	20 sec to 40 sec
Thermal Resistance Junction-to-Ambient[3]	
θ_{JA}, MSOP – 10	216°C/W
θ_{JA}, LFCSP - 10	41°C/W
Package Power Dissipation	(T_J max – T_A)/θ_{JA}

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Includes programming of OTP memory.
[3] Thermal Resistance (JEDEC 4 layer(2S2P) board).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

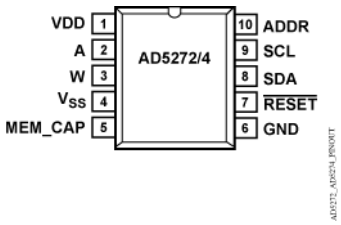

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$
3	W	Wiper terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$
4	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
5	MEM_CAP	Connect a 1µF capacitor between MEM_CAP and V_{SS}.
6	GND	Ground Pin, Logic Ground Reference.
7	$\overline{\text{RESET}}$	Hardware reset pin. Refreshes the RDAC register with the contents of the 50-TP memory register. Factory default loads midscale until the first 50-TP wiper memory location is programmed. $\overline{\text{RESET}}$ is active low. Tie $\overline{\text{RESET}}$ to V_{DD} if not used.
8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input registers. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
9	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input registers.
10	ADDR	Three-State Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 6).

THEORY OF OPERATION

The AD5272 and AD5274 digital programmable resistors are designed to operate as true variable resistors for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The resistor wiper position is determined by the RDAC register contents. The RDAC register acts as a scratchpad register which allows unlimited changes of resistance settings. The RDAC register can be programmed with any position setting using the I²C interface. Once a desirable wiper position is found, this value can be stored in a 50-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of 50-TP data takes approximately TBDms; during this time, the AD5272/4 will be locked and will not acknowledge any new command preventing any changes from taking place. The acknowledge bit can be polled to verify that the fuse program command is complete.

The AD5272/4 also feature a patented (filed, not yet issued) 1% end-to-end resistor tolerance. This simplifies precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

SERIAL DATA INTERFACE

The AD5272/4 have 2-wire I²C-compatible serial interfaces. These devices can be connected to an I²C bus as a slave device, under the control of a master device. See Figure 2 for a timing diagram of a typical write sequence.

The AD5272/4 support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The AD5272/4 each have a 7-bit slave address. The five MSBs are 01011 and the two LSBs are determined by the state of the ADDR pin. The facility to make hardwired changes to ADDR allows the user to incorporate up to three of these devices on one bus as outlined in Table 6.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address and a R/W bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

INPUT SHIFT REGISTER

For the AD5272/4 the input shift register is 16 bits wide (Figures 3 and 4). The 16-bit word consists of two unused bits (should be set to zero), followed by four control bits, and ten DAC data bits, for the AD5274 the lower 2 DAC data bits are don't cares if the RDAC register is read from or wrote to. Data is loaded MSB first (Bit 15). The four control bits determine the function of the software command (Table 7). Figure 2 shows a timing diagram of a typical AD5272/4 write sequence.

The command bits (Cx) control the operation of the digital potentiometer and the internal 50-TP memory. The data bits (Dx) are the values that are loaded into the decoded register.

Table 6. Device Address Selection

ADDR	A1	A0	7-Bit I²CDevice Address
GND	1	1	0101111
V_{DD}	0	0	0101100
NC (No Connection)[1]	1	0	0101110

[1] Not available in bipolar mode. VSS < 0V

WRITE OPERATION

It is possible to write data which for the RDAC register or the control register. When writing to the AD5272/AD5274, the user must begin with a start command followed by an address byte ($R/\overline{W} = 0$), after which the AD5272/4 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the DAC, the most significant byte followed by the least significant byte both of these data bytes are acknowledged by the AD5272/AD5274. A stop condition follows. The write operations for the AD5272/4 are shown in Figure 6 and Figure 7.

A repeated write function gives the user flexibility to update the device a number of times after addressing the part only once(see Figure 8)

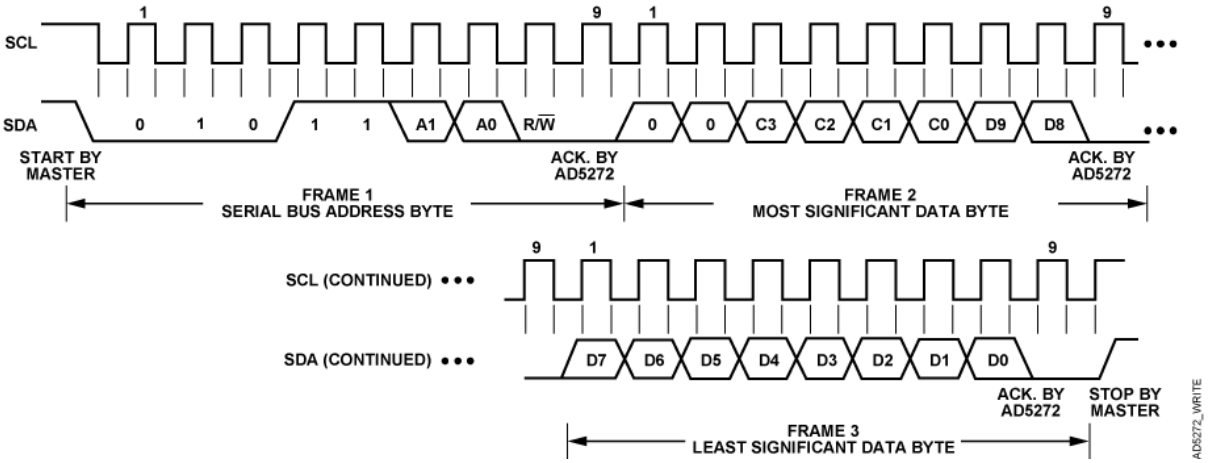

Figure 6. AD5272 Interface Write Command

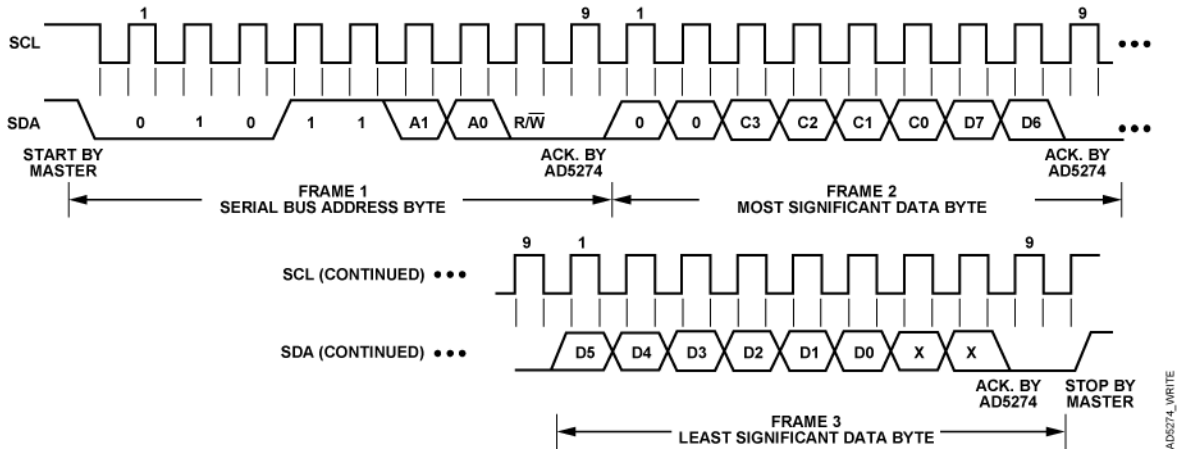

Figure 7. AD5274 Interface Write Command

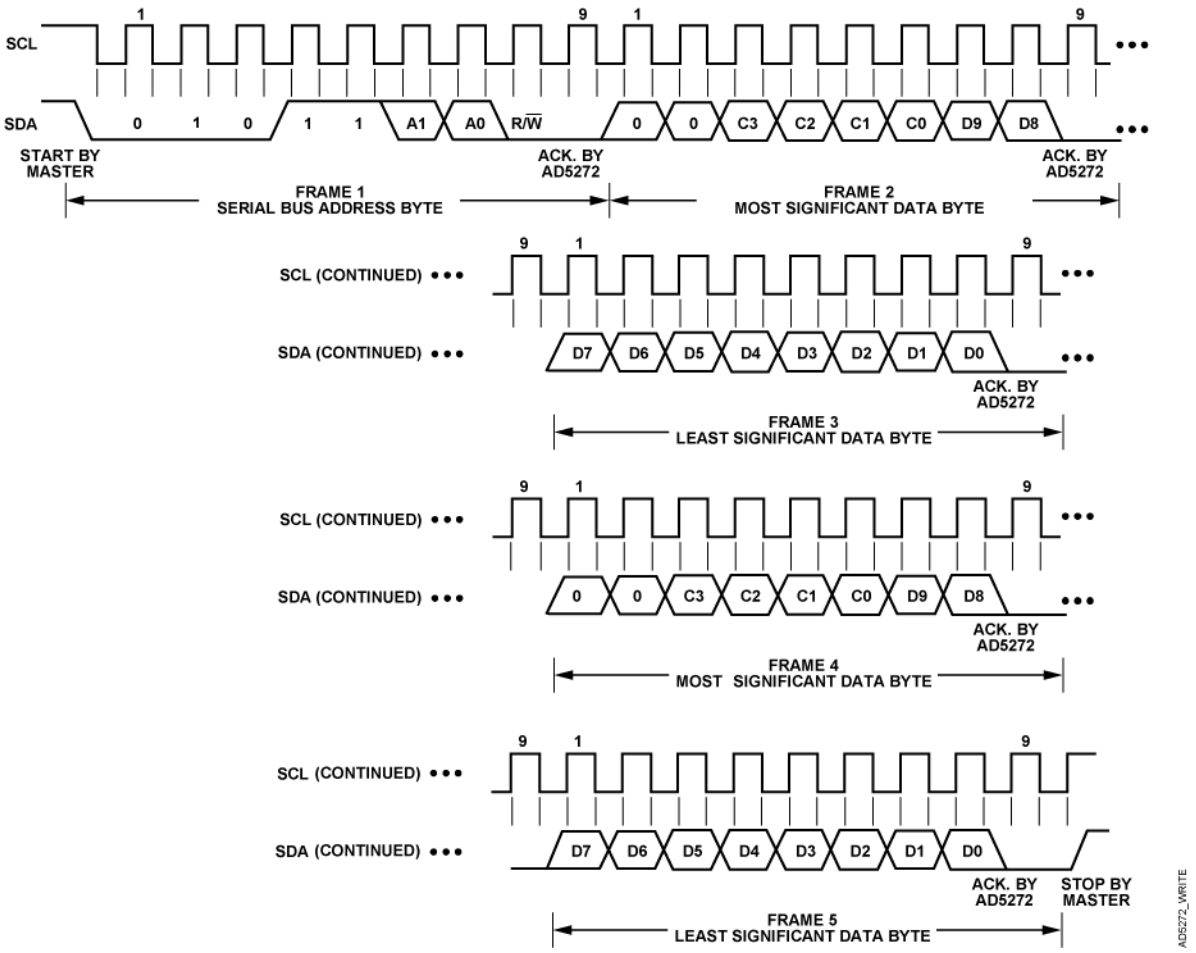

Figure 8 AD5272 Interface Multiple Write

READ OPERATION

When reading data back from the AD5272/4, the user must first issue a readback command to the device, this begins with a start command followed by an address byte ($R/\overline{W}$ = 0), after which the AD5272/4 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the AD5272/4, the most significant byte followed by the least significant byte both of these data bytes are acknowledged by the AD5272/AD5274. A stop condition follows. These bytes contain the read instruction which enables readback of the RDAC register, 50-TP Memory or the control register. The user can then readback the data, this begins with a start command followed by an address byte ($R/\overline{W}$ = 1), after which the device acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the device as shown in Figure 8. A stop condition follows. If the master does not acknowledge the first byte then the second byte is not transmitted by the AD5272/4.

The AD5272/4 does not support repeat read back.

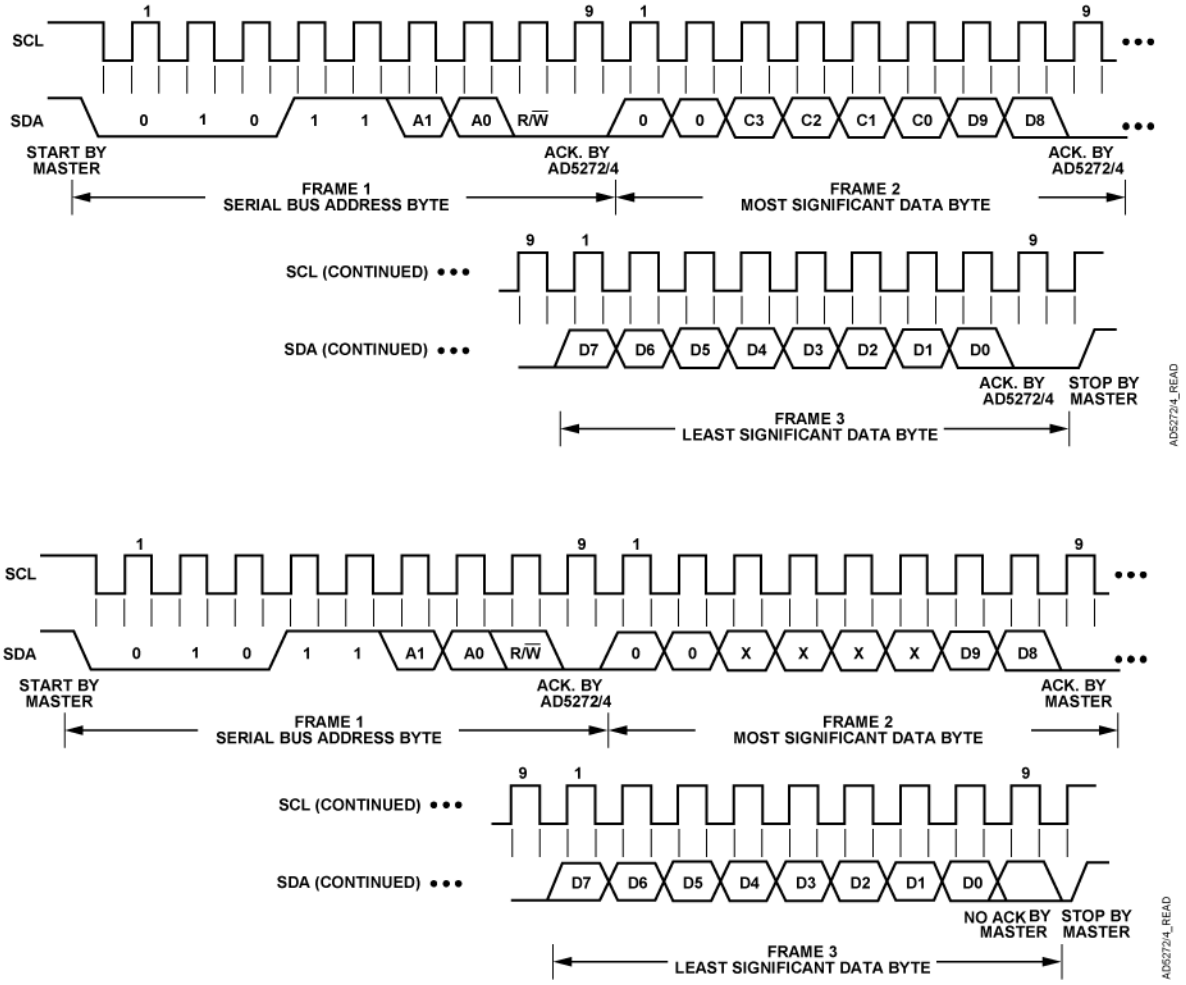

Figure 8 AD5272/4 Interface Read Command

RDAC REGISTER

The RDAC register directly controls the position of the digital rheostat wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal A of the variable resistor. It is possible to both write to and read from the RDAC register using the I²C interface. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

50-TP MEMORY BLOCK

The AD5272/74 contain an array of 50 OTP(One-Time Programmable) memory words which allow the wiper position to be programmed up to 50 times. Table 9 shows the memory map. Once a desirable wiper position is found, this value can be saved into a 50-TP memory register. Thereafter the wiper position will always be set at that position for any future ON-OFF-ON power supply sequence. Command 3, Table 7, is used to program the contents of the RDAC register to memory. The first address to be programmed is location 0x01(see Table 9) and the AD5272/4 increments the 50-TP memory address for each subsequent program until the memory is full. It is possible to read back the contents of any of the 50-TP memory registers through the I²C interface by using Command #5 (Table 7). The lower 6 LSB bits, (D0 to D5) of the data byte, select which memory location is to be read back.

A binary encoded version address of the most recently programmed wiper memory location can be read back using Command #6 (Table 7). This can be used to monitor the spare memory status of the 50-TP memory block.

WRITE PROTECTION

On power-up, serial data input register write commands for both the RDAC register and the 50-TP memory registers are disabled. The RDAC write protect bit, C1 of the control register (Table 8), is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 50-TP memory using the software reset command (Command #4) or through hardware by the $\overline{\text{RESET}}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register) the write protect bit C1 of the control register must first be programmed. This is accomplished by loading the serial data input register with Command #7 (Table 7). To enable programming of the 50-TP memory block bit C0 of the control register, set to 0 by default, must first be set to '1'.

50-TP MEMORY WRITE-ACKNOWLEDGE POLLING

After each write operation to the 50-TP registers, an internal write cycle begins. The I²C interface of the device is disabled. To determine if the internal write cycle is complete and the I²C interface is enabled, interface polling can be executed. I²C interface polling can be conducted by sending a start condition, followed by the slave address and the write bit. If the I²C interface responds with an ACK, the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, I²C interface polling can be repeated until it succeeds.

RESET

The AD5272/AD5274 can be reset through software by executing command 4(Table 7) or through hardware on the low pulse of the $\overline{\text{RESET}}$ pin. The reset command loads the RDAC Register with the contents of the most recently programmed 50-TP memory location. The RDAC Register will be loaded with midscale if no 50-Tp memory location has been previously programmed. Tie $\overline{\text{RESET}}$ to V_{DD} if not used.

SHUT-DOWN MODE

The AD5272/AD5274 can be shut down by executing the software shut down command, command 9 (Table 7), and setting the LSB to '1'. This feature places the RDAC in a zero-power-consumption state where Terminal Ax is open-circuited while the Wiper Terminal Wx remains connected. It is possible to execute any command from Table 7 while the AD5272/AD5274 are in shut down mode. The part can be taken out of shut-down mode by executing command 9 and setting the LSB to '0' or by issuing a software or hardware reset.

Table 7. Command Operation Truth Table

Command Number	Command				Data										Operation
	B13				B9			B8	B7					B0	
	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP: Do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Write contents of Serial Register Data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read contents of RDAC wiper register.
3	0	0	1	1	X	X	X	X	X	X	X	X	X	X	Store Wiper Setting: Store RDAC setting to 50-TP.
4	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Software Reset: Refresh RDAC with last 50-TP memory stored value.
5[1]	0	1	0	1	X	X	X	X	A5	A4	A3	A2	A1	A0	Read contents of 50-TP memory address. Binary address specified by setting bits A5-A0(See Table 9)
									<	<	<	<	ADDR	> > > >	
6	0	1	1	0	X	X	X	X	X	X	X	X	X	X	Read address of last 50-TP programmed memory location
7	0	1	1	1	X	X	X	X	X	X	D3	D2	D1	D0	Write Contents of Serial Register Data to Control Register
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	Read contents of Control Register
9	1	0	0	1	X	X	X	X	X	X	X	X	X	D0	Software Shutdown D0 = 0; Normal Mode D0 = 1; Device placed in Shutdown mode

Table 8. Control Register and special function codes

Register Name	Data Byte D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	Operation
Control	X X X X X X C3 C2 C1 C0	C0 = 50-TP Program Enable 0 = 50-TP program disabled(Default) 1 = Enable device for 50-TP program C1 = RDAC Register Write Protect. 0 = Wiper position frozen to value in OTP memory(Default)[2] 1 = Allow update of wiper position through Digital Interface C2 = Calibration Enable. 0 = RDAC Resistor Tolerance Calibration enabled(Default) 1 = RDAC Resistor Tolerance Calibration disabled C3 = 50-Tp Memory Program Success Bit. 0 = Fuse program command unsuccessful(Default) 1 = Fuse program command successful

[1] See Table 11 for OTP Memory Map
[2] Wiper position frozen to value last programmed in 50-TP memory. Wiper will be frozen to mid-scale if 50-TP memory has not been previously programmed

Table 9. Memory Map

Command Number	Data Byte (ADDR) D9 D8 D7 D6 A5 A4 A3 A2 A1 A0	Register Contents
5	X X X X 0 0 0 0 0 0	Reserved
	0 0 0 0 0 1	1st programmed wiper location[1] (0X01)
	0 0 0 0 1 0	2nd programmed wiper location[1] (0X02)
	0 0 0 0 1 1	3rd programmed wiper location[1] (0X03)
	0 0 0 1 0 0	4th programmed wiper location[1] (0X04)
	0 0 0 1 0 1	5th programmed wiper location[1] (0X05)
	0 0 0 1 1 0	6th programmed wiper location[1] (0X06)
	0 0 0 1 1 1	7th programmed wiper location[1] (0X07)
	0 0 1 0 0 0	8th programmed wiper location[1] (0X08)
	0 0 1 0 0 1	9th programmed wiper location[1] (0X09)
	0 0 1 0 1 0	10th programmed wiper location[1] (0X0A)
	0 1 0 1 0 0	20th programmed wiper location[1] (0X14)
	0 1 1 1 1 0	30th programmed wiper location[1] (0X1E)
	1 0 1 0 0 0	40th programmed wiper location[1] (0X28)
	1 1 0 0 1 0	50th programmed wiper location[1] (0X32)

[1] AD5272, 10-bit wiper memory register; AD5274, 8-bit wiper memory register

RDAC ARCHITECTURE

In order to achieve optimum cost performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5272/4 employs a 3-stage segmentation approach as shown in Figure 9. The AD5272/4 wiper switch is designed with the transmission gate CMOS topology.

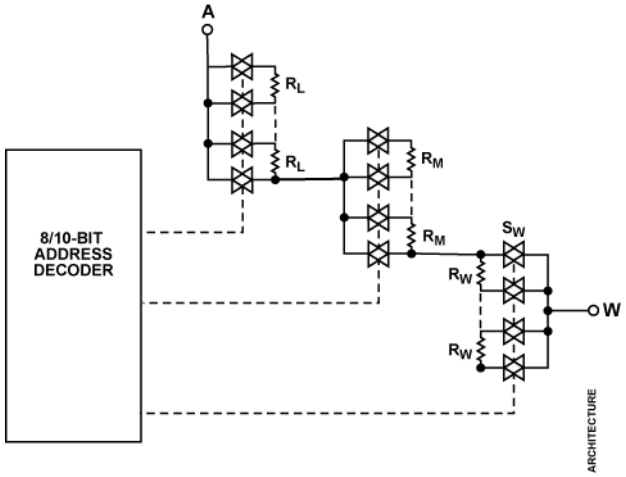

Figure 9. AD5272/4 Simplified RDAC Circuit.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation - 1% Resistor Tolerance

The nominal resistance between Terminal W and Terminal A, R_{WA}, is available in 20 kΩ, 50 kΩ, and 100 kΩ and has 1,024/256 tap points accessed by the wiper terminal. The 10/8-bit data in the RDAC latch is decoded to select one of the 1,024/256 possible wiper settings. The AD5270/1 contain an internal ±1% resistor tolerance calibration feature which can be disabled or enabled, enabled by default, by programming bit C2 of the control register (Table 8). The digitally programmed output resistance between the W terminal and the A terminal, R_{WA} is calibrated to give a maximum of ±1% absolute resistance error over both the full supply and temperature ranges. As a result, the general equations for determining the digitally programmed output resistance between the W terminal and A terminal are AD5272:

$$R_{WA}(D) = \frac{D}{1{,}024} \times R_{WA} \qquad (1)$$

AD5274:

$$R_{WA}(D) = \frac{D}{256} \times R_{WA} \qquad (2)$$

where:
D is the decimal equivalent of the binary code loaded in the 10/8-bit RDAC register.
R_{WA} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of TBD Ω is present. Regardless of which setting the part is operating in, care should be taken to limit the current between the A terminal to B terminal, W terminal to A terminal, and W terminal to B terminal, to the maximum continuous current of ±3 mA(20KΩ) or ±2 mA(50KΩ and 100 KΩ) or pulse current of TBD mA. Otherwise, degradation, or possible destruction of the internal switch contact, can occur.

MEM_CAP CAPACITOR

A 1µF capacitor to V_{SS} must be connected to the MEM_CAP pin (Figure 10) on power-up and throughout the operation of the AD5270/1.

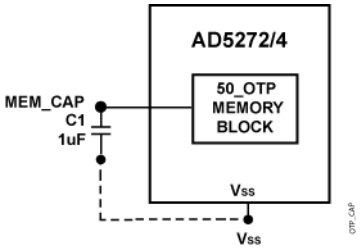

Figure 10 MEM_CAP Hardware Setup

TERMINAL VOLTAGE OPERATING RANGE

The AD5272/4's positive V_{DD} and negative V_{SS} power supplies define the boundary conditions for proper 2-terminal digital resistor operation. Supply signals present on Terminals A and W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (Figure 11).

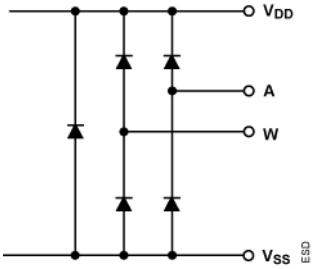

Figure 11 Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5272/4 devices is primarily used as a digital ground reference. To minimize the digital ground bounce, the AD5272/4 ground terminal should be joined remotely to the common ground. The digital input control signals to the AD5272/4 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the Specifications section. An internal level-shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

Power-Up Sequence

Because there are diodes to limit the voltage compliance at Terminals A and W (Figure 11), it is important to power V_{DD}/V_{SS} first before applying any voltage to Terminals A and W. Otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. The ideal power-up sequence is GND, V_{DD}/V_{SS}, digital inputs, and V_A and V_W. The order of powering V_A, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Once V_{DD} is powered, the power-on preset activates, which first sets the RDAC to midscale and then restores the last programmed 50-TP value to the RDAC register.

OUTLINE DIMENSIONS

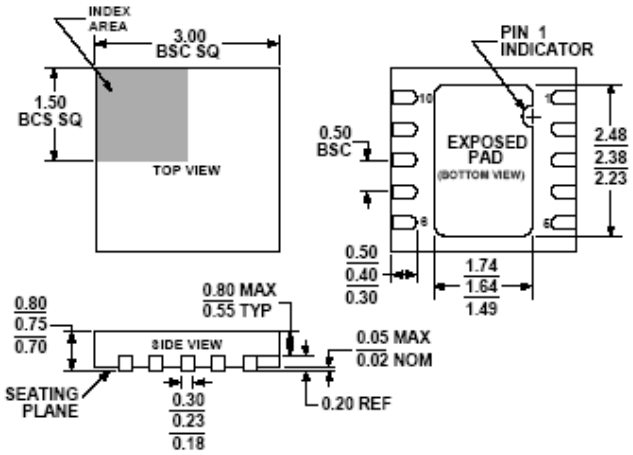

Figure 12. 10-Lead Frame Chip Scale Package[LFCSP_WD]

3mm x 3mm Body, Very Thin, Dual Lead (CP-10-9)

Dimensions shown in millimeters

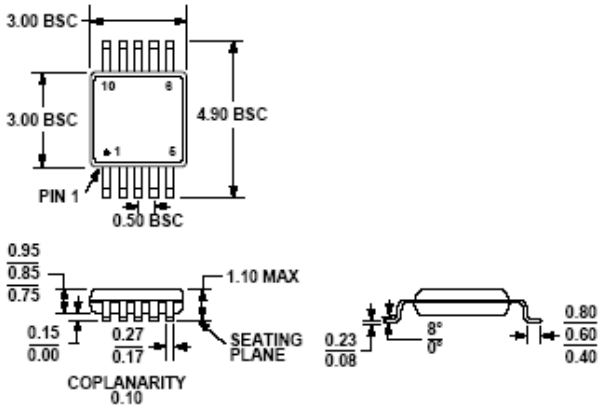

Figure 13. 10-Lead Mini Small Outline Package[MSOP]

(RM-10)

Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (kΩ)	Resolution	Temperature Range	Package Description	Package Option
AD5272BCPZ100-R2	100	1,024	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ100-RL7	100	1,024	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ20-R2	20	1,024	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ20-RL7	20	1,024	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ20-U1	20	1,024	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BRMZ100	100	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ100-RL7	100	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ20	20	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ20-RL7	20	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ-20-U1	20	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ50	50	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ50-RL7	50	1,024	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BCPZ100-R2	100	256	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ100-RL7	100	256	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ20-R2	20	256	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BCPZ20-RL7	20	256	−40°C to +105°C	10-Lead LFCSP_WD	CP-10-9
AD5272BRMZ100	100	256	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ100-RL7	100	256	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ20	20	256	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ20-RL7	20	256	−40°C to +105°C	10-Lead MSOP	RM-10
AD5272BRMZ-20-U1	20	256	−40°C to +105°C	10-Lead MSOP	RM-10

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